Leakage Current Analysis for Diagnosis of Bridge Defects in Power-Gating Designs

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***Abstract*—Manufacturing defects that do not affect the functional operation of low power Integrated Circuits (ICs) can nevertheless impact their power saving capability. We show that stuck-ON faults on the power switches and resistive bridges between the power networks can impair the power saving capability of power-gating designs. For quantifying the impact of such faults on the power savings of power-gating designs, we propose a diagnosis technique that targets bridges between the power networks. The proposed technique is based on the static power analysis of a power-gating design in stand-by mode and it utilizes a novel on-chip signature generation unit, which is sensitive to the voltage level between power rails, the measurements of which are processed off-line for the diagnosis of bridges that can adversely affect power savings. We explore, through SPICE simulation of the largest IWLS'05 benchmarks synthesised using a 32 nm CMOS technology, the trade-offs achieved by the proposed technique between diagnosis accuracy and area cost and we evaluate its robustness against process variation. The proposed technique achieves a diagnosis resolution that is higher than 98.6% and 97.9% for bridges of $R \gtrsim 10M\Omega$ (weak bridges) and bridges of $R \lesssim 10M\Omega$ (strong bridges), respectively, and a diagnosis accuracy higher than 94.5% for all the examined defects. The area overhead is small and scalable: it is found to be 1.8% and 0.3% for designs with 27K and 157K gate equivalents, respectively.**

***Index Terms*—power gating, diagnosis, bridging faults, stuck-ON faults, fault grading**

I. Introduction

Diagnosis of defects is necessary for silicon debugging, yield analysis, and for improving the subsequent manufacturing cycles. Power-gating assures the viability of electronic devices at sub-100-nm CMOS technologies [1] by enabling them to operate in a low-power mode i.e., *stand-by*, during periods of inactivity. The stand-by mode is implemented by embedding power switches together with the on-chip power delivery system for disconnecting the power supply on-demand. Although techniques are available for the diagnosis of defects in power switches, they neglect the on-chip power delivery system, which can be under-designed for low-power mobile applications due to strict time-to-market constraints [2]. Therefore, a systematic technique is required for the diagnosis of defects in power-gating designs that are associated with the on-chip power networks as well as for quantifying their impact on the power-saving capability of their stand-by mode.

Power-gating, which is implemented using either header power switches (pMOS sleep transistors) on the supply power rail V_{dd} or footer power switches (nMOS sleep transistors) on the ground power rail V_{ss} of the power-gated block, has been targeted by testing and diagnosis techniques before [3]–[11]. These techniques target the stuck-open transistor fault model on the power switches that are utilized for disconnecting the virtual supply rail V_{Vdd} or the virtual ground rail V_{Vss}, respectively, during stand-by. Also, diagnosis techniques of defects in power switches [12], [13] focus on evaluating the impact of faults on the power integrity and the performance of the logic that is power gated.

The under-designing of on-chip power delivery systems due to strict time-to-market constraints [2] can impose risks not only to power integrity, but also to the power-saving capability of power-gating designs. For example, defects that are associated with the limited quality of on-chip virtual power networks, such as bridging faults between power rails, can affect the power consumption of power-gating designs without affecting their power integrity and might not be detectable by power-gating testing schemes that do not consider power consumption. When devices that are power gated suffer from defects that affect their power-saving capability at stand-by, power-constraints violations can occur in the systems that contain them. Hence, it is crucial to develop the design-for-testability circuitry and the fault models for testing and diagnosing the power-saving capability of power-gating designs. It would also allow designers to screen out dies with defective stand-by operating mode as well as to quantify the impact of defects on their power-saving capability. This property would allow the ranking of dies and their binning to markets of IC applications not only according to their speed [14], but also based on their power-saving capability.

In this paper, we demonstrate that defects that do not affect the functionality or the performance of power-gating designs can impair their power-savings at stand-by and we propose a diagnosis technique for quantifying the severity of such defects. In particular, we consider bridging faults between the power rails, which as shown in Section II are likely to occur in power-gating designs. In Section II, we also examine whether the power-savings achieved by power-gating designs during periods of inactivity is affected by stuck-ON faults on the power switches and resistive bridging faults between the power rails, and we demonstrate, through SPICE simulation, that either a single faulty power switch or a weak resistive

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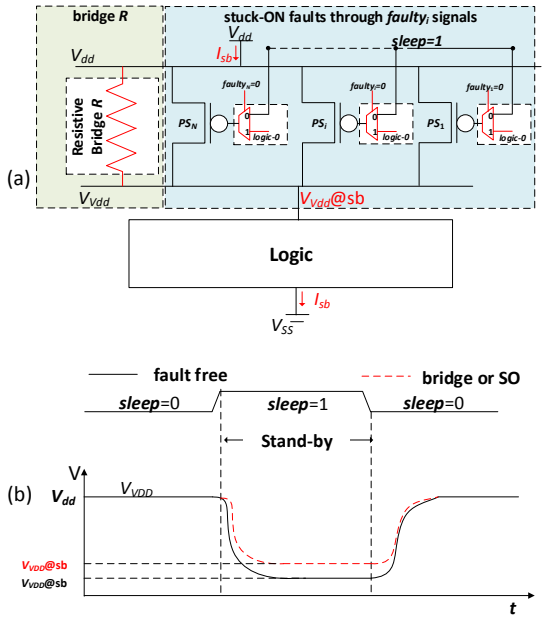

Fig. 1. (a) Power gating with header power switches and fault injection mechanism for resistive bridges and stuck-ONs; (b) impact of faults on the V_{Vdd} during the transition power-on→stand-by→power-on mode.

bridging fault between power rails V_{Vdd} and V_{dd} are enough to impair the power-saving capability of power-gating designs. In Section III, we propose a diagnosis technique of bridges between the power rails, which is based on the static power analysis of the design at stand-by. The proposed technique utilizes a novel low-cost on-chip signature generation unit, which is sensitive to the voltage between the power-rails. The measurements of the sensor are combined with the static power data by a novel diagnosis algorithm that evaluates the bridge between the power rails V_{Vdd} and V_{dd} at stand-by as well as its impact on the power-savings. The sensor can be calibrated for handling uncertainty induced by model-to-silicon discrepancies and process variation. In Section IV, through SPICE simulation of the largest IWLS'05 benchmarks [15] synthesized using a 32 nm technology, we evaluate the trade-offs achieved by the proposed technique between diagnosis accuracy, resolution and area overhead and we show that it achieves higher than 98.6% and 97.9% diagnosis resolution, on bridges $R \gtrsim 10\ M\Omega$ (weak bridges) and bridges $R \lesssim 10\ M\Omega$ (strong bridges), respectively, with a diagnosis accuracy greater than 94.5%. The area overhead is small and scalable: it is found to be 1.8% and 0.3% for designs with 27K and 157K gate equivalents, respectively. The robustness of the proposed technique against process variation is also evaluated. In Section V, conclusions are drawn.

II. Static Power Analysis of Power-Gating Designs with Stuck-ON and Bridging Faults

In this section, we review power-gating with header power switches and we conduct a static power analysis on power-gating designs with faults that do not affect their functionality, but are expected to impact their power saving capability. We examine stuck-ON faults on the power switches and resistive bridges between the power supply networks.

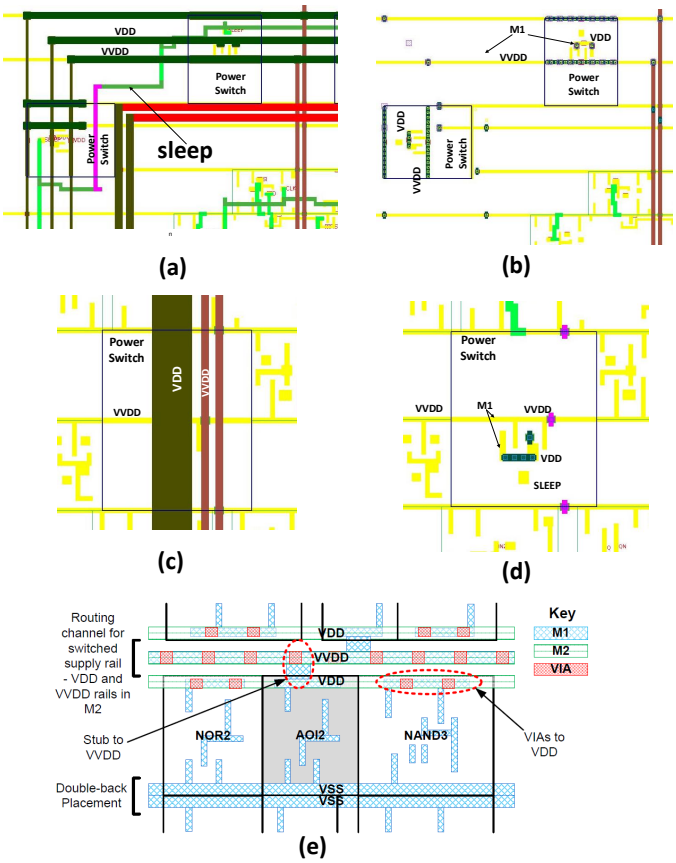

Fig. 2. Power rails and vias at the physical layout of power-gating design practices that can suffer by bridges: (a),(b) ring-style power gating; (c),(d) grid-style power gating; (e) industrial practice of dRing power-gating. ((a)(b)(c)(d) are obtained from physical synthesis and (e) is reproduced from [16]).

A. Power-gating overview and the setup for injection of faults

The power-gating general scheme consists of header power switches is shown in Figure 1(a). The power supply V_{dd} is disconnected from the virtual power supply V_{Vdd} during periods of inactivity in order to reduce the static power consumption of the circuit. This operation, which is shown in Figure 1(b), is performed by asserting the *sleep* signal of the power switches and is followed by a considerable voltage drop of the V_{Vdd}. Therefore, in stand-by mode, the static power consumption is minimum.

Bridges are injected by including a resistance R between the V_{dd} and the V_{Vdd}. For a fault-free simulation the value of R is set to $R = 1\ G\Omega$, a value which is high enough to emulate the IR-drop of the fault-free case, when R is not present. For injecting stuck-ON faults on the power switches, a multiplexer is connected to the gate of each power switch. A $faulty_i$ signal controls whether a power switch PS_i remains ON during the stand-by mode.

In order to motivate the consideration of a bridging fault model between the power rails, we present in Figure 2 the layout of three power-gating design approaches and we highlight critical areas that may be affected by bridge defects, especially if the on-chip power rails are of limited quality, as discussed in Section I. These layouts, except the one presented in Figure 2(e), have been generated using Synopsys IC Compiler. In

the ring-style power-gating (Figures 2(a)(b)), where the power switches are placed at the boundary of the design, the rails V_{Vdd} and V_{dd} stand adjacent to each other at higher metal layers (Figures 2(a)), which is also supported by [17], thus a resistive bridge defect is possible to occur. Also, vias that connect the two rails (Figures 2(b)) from the higher metals to the power switches pins are required. Inevitably, the area of the power switches can become congested and critical for bridge defects due to vias, rails and nets. This issue also affects the grid style power-gating approach (Figure 2(c)(d)), where the power switches are spread in the power-gating design. Although the two power rails might not be adjacent at higher metal layers (Figure 2(c)) in that case, they inevitably reach the pins of the power switches through vias which are adjacent, as shown in Figure 2(d), therefore a bridge defect is possible to occur there. Next in the dRing approach [16] (Figure 2(e)), where power-gating logic co-exists with voltage islands, the two rails are adjacent at the very low metal layers and bridge defects can appear there too. Another approach, where the two rails can be adjacent more frequently within a power switch is the fine-grained power-gating [18], where a power switch is integrated with each logic cell. Finally, a bridging fault model between the V_{Vdd} and the V_{dd} power rails does not model only possible direct bridges between the two rails, but also any indirect bridges, such as bridges of the rail V_{Vdd} with logic nets that are at logic-high value. Therefore, the practicality of a bridging fault model can also be used for the diagnosis of bridges between the virtual rail and the sleep signal, which is also routed close to the V_{Vdd} rail, as shown in Figure 2(a).

Finally, we note that all circuits in this paper have been synthesized using a 32 nm high-k metal gate CMOS technology [19]. The reason for targeting high-k technologies is that these technologies are necessary for low power designs below 65 nm [20], because they manage to successfully minimize the gate leakage current. As a result, the sub-threshold leakage becomes their major leakage component, which is successfully tackled by utilizing power-gating.

B. DC Analysis of Bridges and stuck-ONs

We examine how possible resistive bridges between the networks of the power supply V_{dd} and the virtual power supply V_{Vdd} affect the static power consumption at stand-by. For this purpose, we conduct DC analysis on the c432 circuit from the ISCAS'85 benchmarks using SPICE. We inject a resistive bridge of resistance R, as shown in Figure 1(a), between the power-networks. We sweep the R value in the range $R \in [10\Omega \ 1G\Omega]$ with a step size 1.E+01. During the DC analysis, we measure the current during stand-by I_{sb} at power supply (Figure 1(a)). Figure 3 depicts the collected measurements of the leakage current during stand-by I_{sb} as a function of the injected bridge resistance R. Each point is labeled according to the relative power consumption increase compared to the leakage current of the fault-free case, simply denoted as relative power consumption RP, which is computed as $RP(case) = I_{sb}(case)/I_{sb}(FF)X$, where FF denotes leakage current of the fault-free case $I_{sb}(FF)$. As an example, we observe that bridges of 100Ω and $10M\Omega$ exhibit $RP = 94834X$ and 58X higher static power at stand-by compared to the fault-free case, respectively. Next, we consider a case with a single stuck-ON faulty power switch, denoted as SO1 case, which is injected with the fault injection mechanism presented in Figure 1(a), and we compute the relative power $RP(SO1)$. It is $RP(SO1) = 90227X$, which is of the same order of magnitude compared to the RP exhibited by a bridge of $R = 100\Omega$.

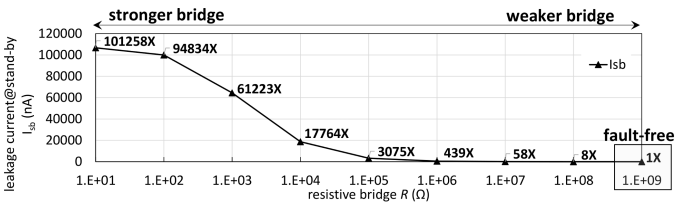

Fig. 3. Leakage current at stand-by I_{sb} obtained by DC analysis and sweeping a resistive bridge R between V_{dd} and V_{Vdd} in the range $R \in [10\Omega, \ 1G\Omega]$

We repeat the DC analysis for a set of the largest IWLS'05 benchmarks [15]. The results are presented in Table I. The first column reports information related to the synthesis of the circuits, such as their size in gate equivalents ge (1 ge is the area of a NAND gate), and the number of power switches utilized (column "ps #"), which is selected to honour an IR-drop less than 10% of V_{dd} constraint. The next two columns report the relative power RP of the fault-free case (column "$RP(FF)$") and the absolute value of the leakage current at stand-by in nA (column "abs."). We note that the reported leakage current includes all possible components and not just the sub-threshold leakage. The next columns that follow report the relative power of the single stuck-ON power

TABLE I
THE BENCHMARK CIRCUITS AND THEIR RELATIVE POWER CONSUMPTION FOR FAULT-FREE AND FAULTY CASES THAT DO NOT AFFECT FUNCTIONALITY

design synthesis			fault-free		RP of stuck-ON faults		RP of resistive bridges		
circuit	size (ge)	ps #	RP(FF)	abs. (nA)	RP(SO1)	RP(SO2)	RP(R=10MΩ)	RP(R=1MΩ)	RP(R=100KΩ)
c432	140	8	1X	1.06	90227X	178552X	58X	439X	3075X
s9234	4190	282	1X	4.04	22716X	45085X	24.2X	221.1X	2045.2X
s5378	4285	302	1X	4.25	21605X	42880X	23.1X	210.4X	1946.1X
s13207	10103	456	1X	5.94	15647X	31066X	17.1X	154.7X	1432.6X
s38584	26864	2609	1X	29.17	3199X	6352X	4.3X	33.1X	301.8X
s38417	30460	3171	1X	34.70	2694X	5350X	3.8X	28X	254.9X
usb_funct	27081	372	1X	5.05	18470X	36681X	20.3X	187X	1739.8X
pci_bridge32	45055	500	1X	6.47	14531X	28860X	16.1X	148.1	1380.9X
ethernet	157520	1956	1X	22.35	4281X	8501X	5.5X	45.4X	415.4X

switch case (column "$RP(SO1)$") and the two stuck-ON power switches case (column "$RP(SO2)$") as well as the relative power of resistive bridges $R = 10M\Omega, 1M\Omega$ and $100K\Omega$ cases. These cases are labeled as "$RP(R = 10M\Omega)$", "$RP(R = 1M\Omega)$" and "$RP(R = 100K\Omega)$", respectively. It is evident that the impact of a single stuck-ON power switch on power consumption at stand-by is 4281X to 90227X higher compared to the fault-free scenarios. At the same time, a minor bridge of $R = 10M\Omega$, which might not even be detectable by stuck-ON testing techniques, induces a 3.8X to 58X higher power consumption compared to the fault-free case. Moreover, bridges of $R = 1M\Omega$ and $R = 100K\Omega$ induce 45.4X to 439X and 415.4X to 3075X higher than the fault-free case power consumption, respectively.

In conclusion, we observe that a single stuck-ON power switch leads to a leakage current at stand-by that is many thousands times higher than the fault-free case, thus impacting the leakage current similarly to a bridge R in the range $[100\Omega\ 10K\Omega]$; even weaker bridges (R=$1M\Omega$) affect the power consumption of the power saving stand-by mode by 45.4X to 439X. Therefore, possible bridges in the extended range between $[100\Omega\ 100M\Omega]$ should be diagnosed for the proper evaluation of the leakage power saving capability of manufactured power-gating designs.

III. Proposed Technique for the Diagnosis of Power-Gating Designs with Bridges

In this section, we present the proposed diagnosis technique for bridges between the power rails of power-gating designs. The proposed technique utilizes a novel low-cost on-chip signature generation unit (Section III-D) based on voltage controlled oscillators (VCOs), which is sensitive to the voltage level of the power-rails. The signatures are processed by an inferencing algorithm (Section III-E), for diagnosing bridges between the power rails V_{Vdd} and V_{dd} at stand-by that affect leakage. A calibration process of the VCOs is also presented in Section III-E2.

A. Proposed technique

We consider the results presented in Figure 3, focusing on how an injected bridge R affects the virtual voltage at stand-by V_{Vdd}@sb. Figure 4(a) depicts V_{Vdd}@sb as a function of the injected bridge resistance R. The scale of 'x'-axis is logarithmic. We emphasize that even minor bridges higher than $100M\Omega$ impact considerably the V_{Vdd}@sb. Next, we consider the leakage current at stand-by I_{sb} as a function of the V_{Vdd}@sb in Figure 4(b) (the 'x'-axis is linear and the 'y'-axis is logarithmic). This correspondence is derived from the data of Figure 3 and Figure 4(a). As a result, it is evident that the leakage current at stand-by is exponentially affected by the virtual voltage at stand-by i.e. V_{Vdd}@sb, a relationship that is analytically explored in the next paragraph. The basic idea of this work is to measure V_{Vdd}@sb in order to diagnose the magnitude of resistive bridges that impact the static power consumption of a power-gating design. For measuring V_{Vdd}@sb on-chip, we propose a power-networks sensor architecture based on voltage-controlled oscillators

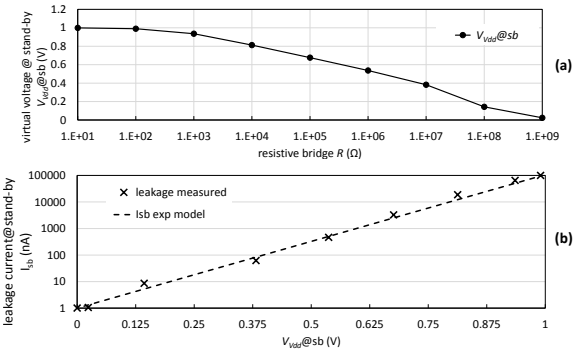

Fig. 4. (a) DC analysis results of V_{Vdd} at stand-by when we sweep a bridge defect between V_{dd} and V_{Vdd}; (b) leakage current I_{sb} is affected exponentially by V_{Vdd}@sb

(VCOs). For the diagnosis of bridges, the collected VCO measurements are processed by a diagnosis algorithm that utilizes the relationship between the static power consumption of a power-gating design at stand-by and V_{Vdd}@sb. This relationship is analytically described next.

B. Analytical model of the leakage current at stand-by

For power-gating designs manufactured using high-k CMOS technologies, the major leakage current component is the sub-threshold I_{st} [20], which is analytically expressed as [21]:

$$I_{st} = I_0 W \cdot e^{\frac{V_{gs}-(V_{t0}-\eta V_{ds}-\gamma V bs)}{nV_T}} \cdot \left[1 - e^{\frac{-V_{ds}}{V_T}}\right] \quad (1)$$

where $I_0 = \frac{\mu_0 C_{ox} V_T^2 e^{1.8}}{L}$, $V_T = \frac{kT}{q}$, V_{t0} is the zero-bias threshold voltage, W is the effective transistor width, L is the effective channel length, n is the subthreshold slope coefficient, C_{ox} is the gate oxide capacitance, μ_0 is the mobility, η is the drain-induced barrier lowering coefficient and γ is the linearized body effect coefficient. Note that at the stand-by mode of a power-gating design (using CMOS technology) either the pMOS or the nMOS devices are in the cut-off region. Therefore, for the analytical evaluation of the leakage current at stand-by I_{sb} in respect to the virtual operating voltage V_{Vdd}, any of the two cases, shown in Figure 5, can be considered leading to the same result. The pMOS device in Figure 5(a) and the nMOS in Figure 5(b) are always in the cut-off region since $V_{gs} < V_t$ for these devices, therefore their leakage current is highest when the drain voltage $V_d = V_{Vdd}$ and $V_d = V_{ss}$, respectively. It should be noted that when $V_{Vdd} < |V_t|$, all transistors are in the cut-off region. Yet even in that case, the voltage observed by DC analysis at the drain V_d tends to be pulled towards the inverted value than the one that is connected to the signal, as observed using SPICE simulation. As a result the values for the pMOS (nMOS) of gate voltage $V_g = V_{Vdd}$ ($V_g = V_{SS}$) and drain voltage $V_d = V_{SS}$ ($V_d = V_{Vdd}$) are considered for analytically estimating the leakage current at stand-by I_{sb} of power-gating designs using equation (1) as a function of the V_{Vdd}:

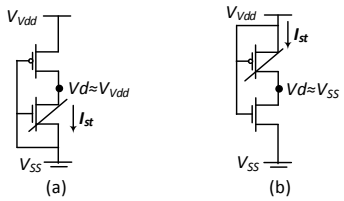

Fig. 5. Possible operating regions of the devices in stand-by mode: (a) pMOS in the cut-off region; (b) nMOS in the cut-off region

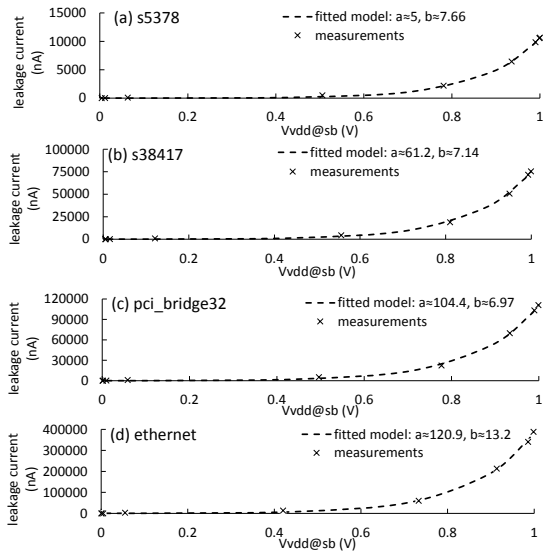

Fig. 6. Fitted models of the I_{sb} for (a) s5378, (b) s38417, (c) pci_bridge32 and (d) ethernet circuits using (2) and SPICE measurements with correlation coefficient values greater than 99.9%

$$I_{sb}(V_{Vdd}) \lesssim I_0 W e^{\frac{\overbrace{V_{gs}}^{0}-(V_{t0}-\eta(V_s-V_{Vdd})-\gamma V_{bs})}{nV_T}}\left[1-e^{\frac{\overbrace{-V_{ds}}^{1}}{V_T}}\right] \Rightarrow$$
$$I_{sb}(V_{Vdd}) \approx a \cdot e^{b \cdot V_{Vdd}} \quad (2)$$

with $a = F_a \cdot I_0 W e^{\frac{-V_{t0}-\eta V_S-\gamma V_{bs}}{nV_T}}$ and $b = F_b \cdot \frac{\eta}{nV_T}$, where F_a, F_b are fitting coefficients used for building a power model using SPICE simulations. The parameter F_a is used to fit the linear impact of the effective transistor width W to the effective transistor length L ratio of the circuit. Similarly, F_b is used to fit the exponential impact of the drain induced barrier lowering effect η. The parameter η is obtained from technology libraries and the ratio is established during the design stage. As expected, the power saving in power-gating designs at stand-by occurs due to an exponential reduction of the subthreshold leakage current with the virtual voltage.

This analytical model enables the static power analysis of power-gating designs at stand-by. To validate this model using our setup, we sweep the bridge R in the range $R \in [10\Omega,\ 1G\Omega]$ and we collect the leakage current measurements and the virtual voltage at stand-by V_{Vdd}@sb, through SPICE simulation. Figure 6 depicts the results using SPICE and the fitted model using (2) of four examined benchmarks of various sizes (Table I). The correlation coefficient between the predictions of the model and the measurements was found

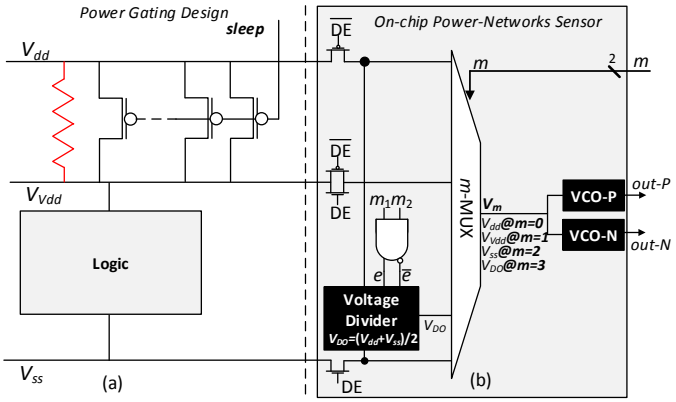

Fig. 7. The on-chip power-networks sensor architecture

in the range [99.93%-99.98%] and the average relative error was in the range [1.3%-5.4%] for the examined benchmarks. The model performs with higher accuracy for larger designs.

C. The on-chip power-networks sensor

The proposed on-chip power-networks sensor for collecting measurements from the voltage level exhibited on the power-networks at stand-by is shown in Figure 7. On the left (Figure 7(a)), the power gating design architecture is shown. The power-networks sensor architecture, shown on the right (Figure 7(b)), consists of two voltage controlled oscillators (VCOs), the VCO-P and VCO-N, that are shared between the power-networks using multiplexer m-MUX. The m determines which power rail is observable by the VCOs. As an example, when $m = 1, 2, 3$ and 4, the rails V_{dd} of the power-supply network, V_{Vdd} of the virtual power-supply network, V_{ss} of the ground network, and V_{DO} of the voltage divider, are observable by the VCOs, respectively. This way only one pair of VCOs are required. V_{DO} is a virtual power rail that is generated by an on-chip voltage divider, which is used for calibrating the VCOs. A pMOS device connected to the V_{dd} power rail, an nMOS device connected to the V_{ss}, and a transmission gate connected to the V_{Vdd} rail (Figure 7(b)) are used for power-gating the proposed architecture during the circuit normal operation by de-asserting the diagnosis enable (DE) signal. The stacking effect of these devices with the on-chip power-networks sensor minimizes any negative impact on the power consumption and performance of the circuit during normal operation. The reasons for using two VCOs is for observing the full voltage spectrum [V_{ss} V_{dd}]. Note that the m signal does not determine the state (power-ON or stand-by) of the power-gating design. It only determines the rail that is observed from the sensor, when the circuit is in diagnosis mode (DE=1). The state of the circuit is determined by the sleep signal. Next, we present in detail the VCO-P, VCO-N and the voltage divider designs:

VCO-P: The VCO-P stage cell is an inverter, shown in Figure 8(a), with the size of the pMOS S_p twice the size of the nMOS S_n ($S_p = 2 \cdot S_n$). The drain of the pMOS is connected to the voltage that is observable (V_m) and the previous stage of the cell is connected to the gate of the devices. The output of

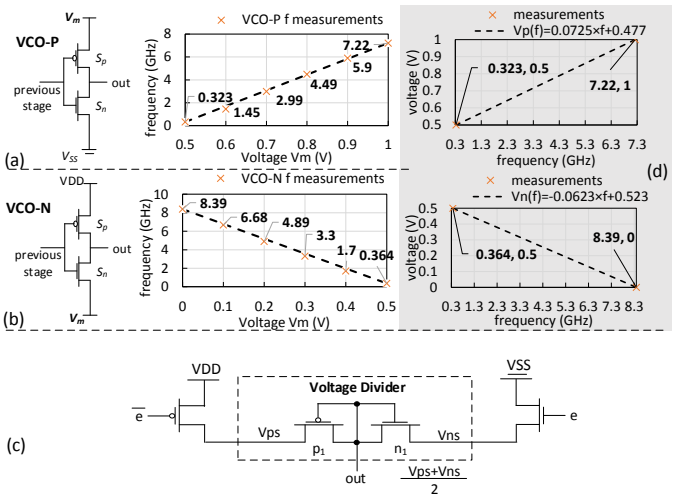

Fig. 8. (a) VCO-P cell; (b) VCO-N cell; (c) low-power voltage divider; (d) characteristics functions of VCOs after calibration

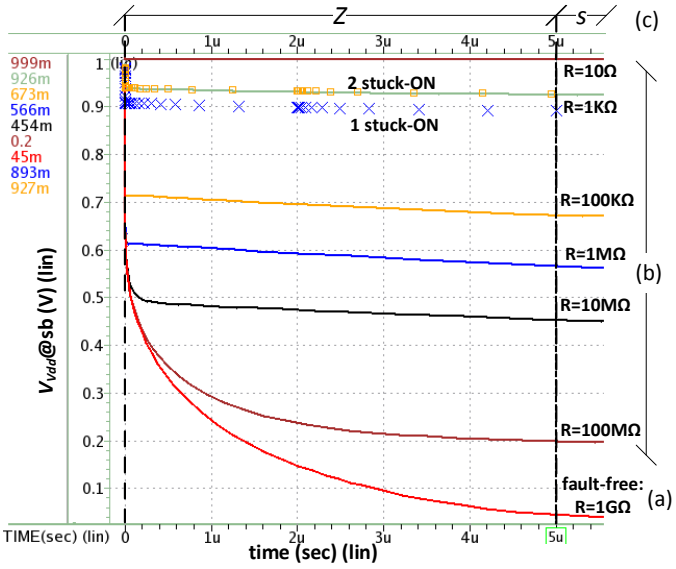

Fig. 9. AC analysis of bridges at power rails and stuck-on power switches

an 11-stage VCO-P is obtained through SPICE simulation for various voltage levels V_m and is shown in Figure 8(a). The VCO-P interacts with voltage V_m in the range $[V_{dd}/2, V_{dd}]$.

VCO-N: Similarly, the VCO-N stage cell is an inverter, shown in Figure 8(b), with the size of the pMOS S_p half the size of the nMOS S_n ($S_p = 0.5 \cdot S_n$). This time, the source of the nMOS is connected at the voltage that is observable (V_m) and the previous stage of the cell is connected at the gate of the devices. The output of an 11-stage VCO-N is obtained through SPICE simulation for various voltage levels V_m and is shown in Figure 8(b). The VCO-N interacts with voltage V_m in the range $[V_{ss}, V_{dd}/2]$.

Voltage divider: This circuitry is shown in Figure 8(c) and it consists of a pMOS and an nMOS in series with $S_p = 0.5 \cdot S_n$. The gates of the devices, the source of the pMOS and the drain of the nMOS are shorted, a feedback that forces the device output to half the voltage difference applied between the drain of the pMOS (V_{dd}) and the source of the nMOS (V_{ss}). This device consumes power when it is activated, therefore, when it is not required, it is power gated using a pMOS power switch on the V_{dd} and an nMOS power switch on the V_{ss}. Note that this device is needed only for calibrating the on-chip VCOs.

Model-to-silicon discrepancies [22] affect simulation results, which might be inaccurate compared to actual hardware measurements due to neglected parasitics or process variation that could affect the voltage-to-frequency functions of the VCOs uniquely for every die. Therefore, the proposed sensor collects measurements from the power-networks and the output of the voltage divider. This data is used for the post-silicon calibration of the VCOs, which is part of the proposed diagnosis algorithm described in Section III-E. Also note that on-chip power network sensors already exist for power noise profiling [23], adaptive systems to power noise [24], trojan detection [25] and monitoring ageing [26]. However, such sensors collect data during the active operating mode of a circuit and not during the stand-by mode of a power-gating design, except [26] which collects data during the transit of the circuit from active to stand-by mode. For the proposed technique, one power-networks sensor is sufficient, because the collection of the signature is performed when the circuit is at the steady-state of the stand-by mode.

D. Signature generation unit

The transition from the active to the stand-by mode is not instantaneous. Its study is crucial for describing the signature generation unit. Hence, the AC analysis of the transition is described in the next paragraph and shown in Figure 9.

1) AC analysis of bridges and stuck-ON power switches: For examining the transient behaviour of the virtual voltage during the transition from active to stand-by mode, we carry out SPICE simulation on the c432 circuit and we conduct AC analysis for 7 different cases by varying the resistive bridge $R = [1G\Omega,\ 100M\Omega,\ 10M\Omega,\ 1M\Omega,\ 100K\Omega,\ 1K\Omega,\ 10\Omega]$. We also examine two cases with a single and two stuck-ON power switches. We set as initial condition of the circuit the wake-up state (sleep=0). Then, at time $t = 1ns$, we assert the sleep signal (sleep=1) and we collect measurements for the next $t = 5usec$. Figure 9 depicts the gathered virtual voltage V_{Vdd}@sb traces. For the fault-free case ($R = 1G\Omega$), we observe that the V_{Vdd}@sb drops below 50mV (Figure 9(a)). We also observe that a bridge of $R = 1M\Omega$ leads to a V_{Vdd}@sb higher than 0.5V.

The signature generation unit consists of the power-networks sensor and a signature generation control logic, shown in Figure 10. The control logic sets the circuit in stand-by mode and utilizes the sensor in order to collect measurements from the VCOs stimulated by every power rail at stand-by. It is controlled by a Finite State Machine (FSM) which coordinates the subsequent components.

2) Signature generation control logic: First, a 2-bit counter, the m-counter, controls the m-MUX for selecting which power rail is monitored by the VCOs. Then, two synchronous counters are used for integrating delay: the stand-by settling time counter (z-counter) and the wait sampling time counter

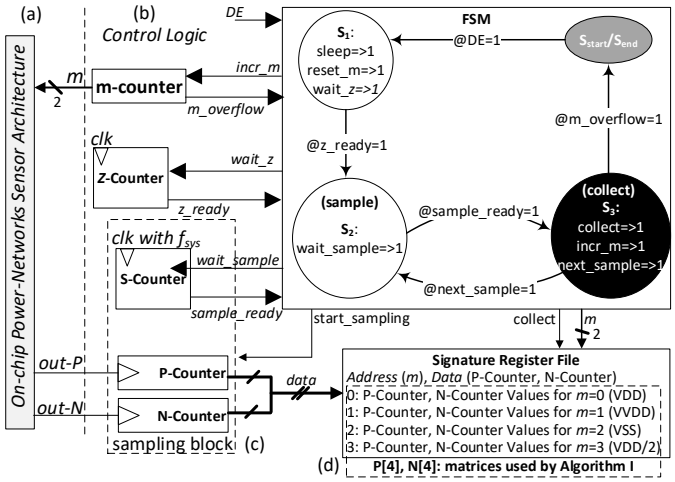

Fig. 10. Signature generation unit: (a) on-chip power-networks sensor; (b) signature generation control logic; (c) sampling block; (d) signature generation file and stored values of P, N-counters

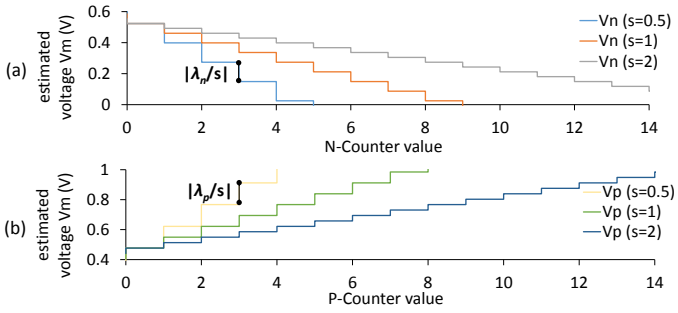

Fig. 11. Estimated voltage and sampling error for sampling times $s = 0.5, 1$ and 2 ns for (a) N-Counter and (b) P-Counter

(s-counter). The settling z-counter is used for delaying the signature generation until the circuit has finished its transition and has settled to the stand-by mode, as shown in Figure 9. The size of the z-counter affects the settling time, denoted by z. The value of z should be large enough to allow the circuit to settle in stand-by mode and it can be estimated using SPICE simulation (Figure 9). Then the size of the z-counter should be chosen to be high enough to guardband any model-to-silicon discrepancies. As an example, a 13-bit synchronous settling z-counter with a system clock frequency $f_{sys} = 1.25\ GHz$ allows for a settling time $z > 6.5\ \mu s$. The considered system clock frequency f_{sys} is for the fastest examined circuit and the resulting settling time z is one order of magnitude higher than the settling time of all the examined circuits. Finally, a register file is used for storing the signature.

3) Sampling block and sampling setup: The s-counter and the N, P counters consist of the *samping block* (SB), shown in Figure 10(c). The s-counter is used for holding the FSM for the sampling time delay s after the circuit has reached steady-state (Figure 9(c)), in which the P, N counters, sample measurements from the VCOs. The s-counter size $|s|$ and the system operating frequency f_{sys} are the *sampling setup* of the sampling block (Figure 10). It is $s = 2^{|s|} \cdot 1/f_{sys}$. Note that the size of the P and N counters, denoted as $|X|$, also depend on the maximum number of clock cycles during the sampling interval s by $|X| = \lceil log_2(s/T_{min}) \rceil$, where T_{min} is the minimum possible oscillation period of the VCOs in the voltage range $[V_{ss},\ V_{dd}]$.

4) Signature generation process: The state diagram of the FSM is shown in Figure 10 and the process for collecting a signature is as follows: the FSM initially is at state S_{start}. The process begins with the assertion of the DE signal. In state S_1, the circuit is set in stand-by mode by asserting the sleep signal and the FSM resets the m-counter. Upon that state, the z-counter is triggered by asserting the wait_z. Upon the z-counter expiration the z_ready signal is asserted and the FSM is informed that the circuit has reached the stand-by mode and is ready for measurements. Then, the FSM is set at state S_2, in which the P and N counters are stimulated/enabled by the outputs of the two VCOs and, hence, they start counting. At the same time, the s-counter starts counting, because the FSM asserts the *wait_sample* signal. The overflow of the s-counter, which is signaled by the assertion of the *sample_ready* signal sets the FSM to the next state, S_3. In that state, the values reached by the P-Counter and the N-Counter are concatenated as a *data* bus and stored in the m address at the register file. Then the m-counter is increased and the process repeats from the state S_2, unless the m-counter overflows, which asserts the *m_overflow*, sets the FSM into the state S_{end}. In that state, the signature is ready in the signature register file.

5) Sampling error: There is a quantization error that affects the resolution of the sensor on measuring voltage, which is introduced by the P-Counter and the N-Counter of the sampling block (SB). Specifically, multiple VCOs ringing frequencies f_i can result in the same counter value $P_i = \lfloor f_i \cdot s \rfloor$ ($N_i = \lfloor f_i \cdot s \rfloor$), if the sampling time s is not sufficiently high (Figure 11). To analyze this error, we consider two successive counter values P_i and P_{i+1} (N_i and N_{i+1}) with $P_i = P_{i+1} - 1$ ($N_i = N_{i+1} - 1$) and using the characteristic functions of the VCOs ($V_p(f_i) = \lambda_p \cdot f_i + b_p$ and $V_n(f_i) = \lambda_n \cdot f_i + b_n$, Figure 8(d)), we get:

$$\begin{aligned} EV_x &= V_x(f_{i+1}) - V_x(f_i) \\ &= \lambda_x / s \end{aligned} \tag{3}$$

where x={p,n}. Therefore, EV_x denotes either the EV_n or the EV_p sampling error of the VCO-N and VCO-P ring oscillator, respectively. The proposed diagnosis algorithm considers this error for estimating the possible range of diagnosed bridge. We will demonstrate in Section IV-A that increasing the sampling time s reduces the sampling error; however, it adversely affects the area cost of the sampling block.

E. Diagnosis algorithm

Algorithm 1 is applied off-line on the collected signature for the diagnosis of the bridge between the power rails V_{Vdd} and V_{dd}. It also evaluates its impact on static power consumption of the power-gating design at stand-by.

1) Pre-processing of Inputs: The algorithm considers as input the signature matrices $P[4]$, $N[4]$ (Figure 10(d)), which are the pairs of values obtained from the P-Counter and the N-Counter during monitoring of the power rail options V_{Vdd}, V_{dd}, V_{ss} and V_{DO}. For simple notation, as an index of

Algorithm 1 Diagnosis Algorithm

Inputs: $P[4], N[4]$: signature matrices
Outputs: R_x: diagnosed effective power-networks resistance
ER: diagnosed resistance maximum error
I_{sb}: the leakage current at stand-by
EI: maximum leakage current error

1: Create $F_p[i] = \lfloor P[i]/s \rfloor$ and $F_n[i] = \lfloor N[i]/s \rfloor$ arrays
2: Calibrate VCOs by generating the frequency to voltage functions $V_p(f_x)$, $V_n(f_x)$ for each VCO, respectively, using: $V_p(f_x) = 0.5 + \lambda_p \cdot (f_x - F_p[V_{DO}])$ with $\lambda_p = (V_{dd} - V_{DO})/(F_p[V_{dd}] - F_p[V_{DO}])$ and $V_n(f_x) = 0.5 - \lambda_n \cdot (f_x - F_p[V_{DO}])$ with $\lambda_n = (V_{ss} - V_{DO})/(F_n[V_{ss}] - F_n[V_{DO}])$
3: Estimate V_{Vdd} using both VCOs: $V_p(F_p[V_{Vdd}])$ and $V_n(F_p[V_{Vdd}])$
4: **if** $V_n \leq V_{DO}$ and $V_p < V_{DO}$ **then**
5: diagnosis: $V_x = V_n;\ x = n$
6: **else**
7: diagnosis: $V_x = V_p;\ x = p$
8: **end if**
9: return $R_x(V_x)$, $ER_x(V_x)$ and $I_{sb}(V_x)$, $EI_x(V_x)$

the signature matrices, the rail option is used. For example $N[V_{DO}]$ is the N counter value, when the voltage divider power rail V_{DO} is monitored. The first step of the Algorithm 1 is to compute the quantized frequency of the VCO-P and VCO-N using $F_p[i] = \lfloor P[i]/s \rfloor$ and $F_n[i] = \lfloor N[i]/s \rfloor$, respectively, where s is the sampling time and F_p and F_n are matrices of size $|F_x| = 4$ elements, one element for each power rail option.

2) Calibration of the VCOs: The next step of the Algorithm 1 tackles any process variation effect on the VCOs (VCO-P and VCO-N). The characteristic functions $V_p(f_x)$ and $V_n(f_x)$ of the VCO-P and VCO-N, respectively, are evaluated using the collected signature. This calibration process, which is shown analytically in Algorithm 1, is conducted by a linear fit to the collected measurements, which is shown, as an example, in Figure 9(d). Particularly, $V_p(f_x)$ is obtained by considering the oscillation frequencies of the power rails V_{DO} and V_{dd}. Similarly, $V_n(f_x)$ is obtained by considering the oscillation frequencies of the power rails V_{SS} and V_{DO}.

3) Diagnosis of effective resistance between V_{Vdd} and V_{dd}: For obtaining the resistance between the V_{dd} and V_{Vdd} rails, we use Ohm's Law on the voltage difference $\Delta V_x = V_{dd} - V_x$, where V_x is the estimated voltage of the V_{Vdd} rail: (2) the following analytical expression, which is derived by applying

$$R_x(V_x) = \Delta V_x / I_{sb}(V_x) \tag{4}$$

where $I_{sb}(V_x)$ is the estimated static power consumption at stand-by given by (2), which has been fitted using data obtained through SPICE simulation. The effective resistance R_x consists of the fault-free effective resistance between the V_{dd} and V_{Vdd} power-networks and any possible bridge R. Therefore, R can be computed using $1/R_x = 1/R + 1/R_{FF}$, where R_{FF} is the expected fault-free effective resistance between the power-networks. In the fault-free case, it is $R_x \simeq R_{FF}$. This property can be used for obtaining the fault-free resistance between V_{dd} and V_{Vdd} networks by collecting data from fault-free dies.

4) Diagnosis estimation range: The sampling voltage error EV_x of the VCOs, also affects the diagnosis resolution, by introducing an estimation error at the diagnosed effective resistance between the power rails. This error, denoted as ER_x, is evaluated by Algorithm 1 analytically using:

$$\begin{aligned} ER_x(V_x) &= \frac{R_x(V_x + EV_x) - R_x(V_x)}{R_x(V_x)} \xRightarrow{(3)\text{ and }(4)} \\ ER_x(V_x) &= \frac{1}{1 + EI_x} \cdot (1 - \frac{EV_x}{\Delta V_x}) - 1 \end{aligned} \tag{5}$$

where $\Delta V_x = V_{dd} - V_x$ and EI_x the relative power estimation error of either the VCO-P or VCO-N:

$$\begin{aligned} EI_x &= \frac{I_{sb}(V_x + EV_x) - I_{sb}(V_x)}{I_{sb}(V_x)} \xRightarrow{(2)} \\ EI_x &= e^{b \cdot \frac{\lambda_x}{s}} - 1 \end{aligned} \tag{6}$$

Based on the diagnosed resistance R_x and its evaluated error ER_x, the diagnosis estimation range for the bridge is obtained as: $[R_x,\ (R_x + |ER_x|)]$, when $ER_x > 0$, and $[(R_x - |ER_x|),\ R_x]$, when $ER_x < 0$. In Figures 12(a) and (b), the absolute diagnosis errors $|ER_n|$ and $|ER_p|$ are presented, respectively. Four sampling setups that perform with a sampling voltage error $EV_x = 1, 2, 4$ and 8 mV are considered. It is evident that $|ER_n|$ is maximized at $V_x = V_{dd}/2 = 0.5$ V, while $|ER_p|$ is maximized at $V_x = V_{dd} = 1$ V.

IV. Evaluation Results

In this section, we evaluate the area overhead, diagnosis accuracy and resolution of the proposed technique. The technique is applied to a set of the largest IWLS circuits [15] that

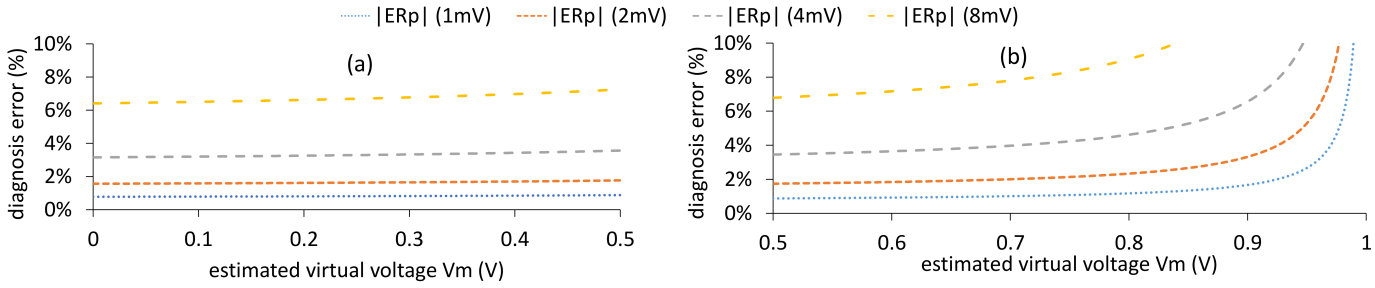

Fig. 12. Expected diagnosis error ER_x when a) $V_{Vdd}@sb \leq V_{dd}/2$; b) $V_{Vdd}@sb > V_{dd}/2$

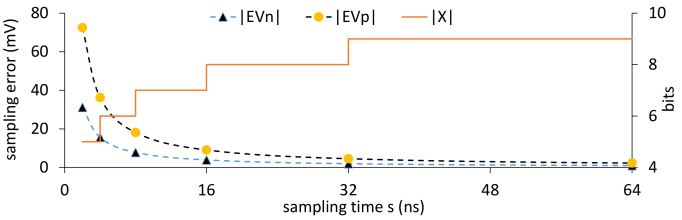

Fig. 13. Trade-off between the absolute sampling voltage errors $|EV_x|$ and the size of P-Counter and N-Counter $|X|$

are synthesized using Synopsys IC compiler and a 32 nm high-k metal-gate CMOS technology [19] with an operating voltage $V_{dd} = 1$ V. SPICE simulation is utilized for the validation of the proposed technique and Monte Carlo for assessing its robustness against process variation.

A. Trade-off between sampling error and area overhead

In the first experiment, we analyze the trade-off between the area overhead of the sampling block and the sampling error. Figure 13 depicts the sampling error EV_x (left 'y'-axis) and the size of P-Counter and N-Counter $|X|$ (right 'y'-axis), as a function of the sampling time s in Figure 13. In order to avoid the overflow of the counters, we consider a period $T_{min} = 0.1$ ns during the selection of their size $|X|$, which is lower than any possible period of the VCOs that drive the counters in the range $[V_{dd},\ V_{ss}]$. Also, we consider a system operating frequency $f_{sys} = 1$ GHz. From Figure 13, it is evident that the sampling error reduces for higher sampling times s, while for $s > 32$ ns both EV_n and EV_p errors are below 1 mV. On the other hand, although we have overestimated $|X|$, we still observe that a sampling error less than 1 mV (for $s \geq 32$ ns) can be achieved with only $|X| = 8$ bits.

B. Area overhead evaluation

The area required by the proposed technique consist of the on-chip power-network sensor, the control logic and the signature register file. The sensor consists of the VCOs, the voltage divider and the transmission gates and it is evaluated as 16 gate equivalents (ge), where a ge the area of a 2-input NAND gate. The control logic (CL) consist of the 4 stages FSM, the 2-bits m-counter, the m-MUX, a 13-bits settling z-counter and the sampling block (SB). Excluding the SB, the CL occupies a constant area of $|CL|$-$|SB|$=124 ge.

The area of the SB, which consist of the S, P and N counters, is affected by the sampling time s providing a trade-off between accuracy and Area overhead (Section IV-A). Also, the size of the signature register file |SRF| depends on $|X|$. It is $|SRF| = 8 \times |X|$ memory bits. Note that the cost of $|SRF|$ can be reduced to $6 \times |X|$ memory bits, because the N[V_{dd}] and P[V_{ss}] values of the signature (Section III-E) are not utilized by the proposed diagnosis Algorithm 1.

We synthesize a set of the largest IWLS circuits [15] together with the proposed signature generation unit and the power-networks sensor for various sampling setups (Section III-D3). The results are presented in Table II. The sampling setup (s,$|s|$) and the operating frequency f_{sys} are shown

TABLE II
SAMPLING BLOCK SETUP, SENSOR SAMPLING VOLTAGE ERROR (EV_x) AND PROPOSED AREA OVERHEAD FOR A SET OF IWLS CIRCUITS

circuit	sampling setup			EV_x(mV)		area overhead (%)	
	f_{sys} (GHz)	$\|s\|$ (bits)	s (ns)	λ_N/s	λ_P/s	AO_{Logic}	AO_{ALL}
s9234	1	4	16	3.9	4.5	5.49	10.64
		5	32	1.9	2.3	5.81	11.61
		6	64	1.0	1.1	6.13	12.58
s5378	1	4	16	3.9	4.5	5.37	10.41
		5	32	1.9	2.3	5.68	11.35
		6	64	1.0	1.1	6.00	12.30
s13207	1.25	4	12.8	4.9	5.7	2.19	4.06
		5	25.6	2.4	2.8	2.32	4.46
		6	51.2	1.2	1.4	2.45	4.86
s38584	1	4	16	3.9	4.5	0.86	1.66
		5	32	1.9	2.3	0.91	1.81
		6	64	1.0	1.1	0.96	1.96
s38417	0.66	4	12.12	5.1	6.0	0.73	1.35
		5	24.24	2.6	3.0	0.77	1.48
		6	48.48	1.3	1.5	0.81	1.61
usb_funct	0.66	4	12.12	5.1	6.0	0.82	1.51
		5	24.24	2.6	3.0	0.87	1.66
		6	**48.48**	**1.3**	**1.5**	**0.92**	**1.81**
pci_bridge	0.66	4	12.12	5.1	6.0	0.49	0.91
		5	24.24	2.6	3.0	0.52	1.00
		6	**48.48**	**1.3**	**1.5**	**0.55**	**1.09**
ethernet	0.5	4	16	3.9	4.5	0.15	0.28
		5	32	1.9	2.3	0.15	0.31
		6	**64**	**1.0**	**1.1**	**0.16**	**0.33**

in the column "sampling setup". In column 'area overhead (%)', we present the area overhead required by the proposed diagnosis technique with respect to the size of the considered circuit. The area overhead, AO_{logic}=$(CL + PNS)/BS$ has been obtained by not including the area of the signature register file SRF. We have, however, accounted for all the logic of the proposed technique, which consists of the control logic CL and the power-networks sensor PNS. BS denotes the benchmark size. The overall area overhead, denoted as AO_{ALL}, is obtained using AO_{ALL}=$(CL+PNS+SRF)/BS$ and accounts also for the SRF area overhead. We highlight that the area overhead of the proposed technique diminishes with the size of the circuit. Particularly, for the largest benchmarks (marked with bold face font in Table II) the overhead is lower than 1.81%, while for the largest one, the ethernet, it is less than 0.33%. The time T_{sg} required by the signature generation process (Section III-D4) to collect the signature from the four power rails (V_{dd}, V_{ss}, V_{Vdd} and V_{DO}) is $T_{sg} = z + 4 \cdot s$, where z is the settling time enforced by the z-counter and s is the sampling time with $z = 2^{|z|}/f_{sys}$. $|z|$ is the size of the z-counter ($|z| = 13$ bits) and f_{sys} is the system clock frequency. For the circuit in Table II with the slowest frequency, it is $T_{sg} < 16.5\ \mu s$. This demonstrates that the proposed technique requires negligible time for collecting a signature.

C. Diagnosis accuracy and resolution evaluation

We validate the proposed technique through SPICE simulation. Specifically, we conduct 400 Monte Carlo (MC) iterations with injected bridge $R_i \leq 1\ G\Omega$ as the random variable. The random bridge is selected to exhibit a virtual voltage at stand-by uniformly distributed in the range $[FF(V_{Vdd}@sb)\ V_{dd}]$, where $FF(V_{Vdd}@sb)$ is the fault-free value of the V_{Vdd}@sb.

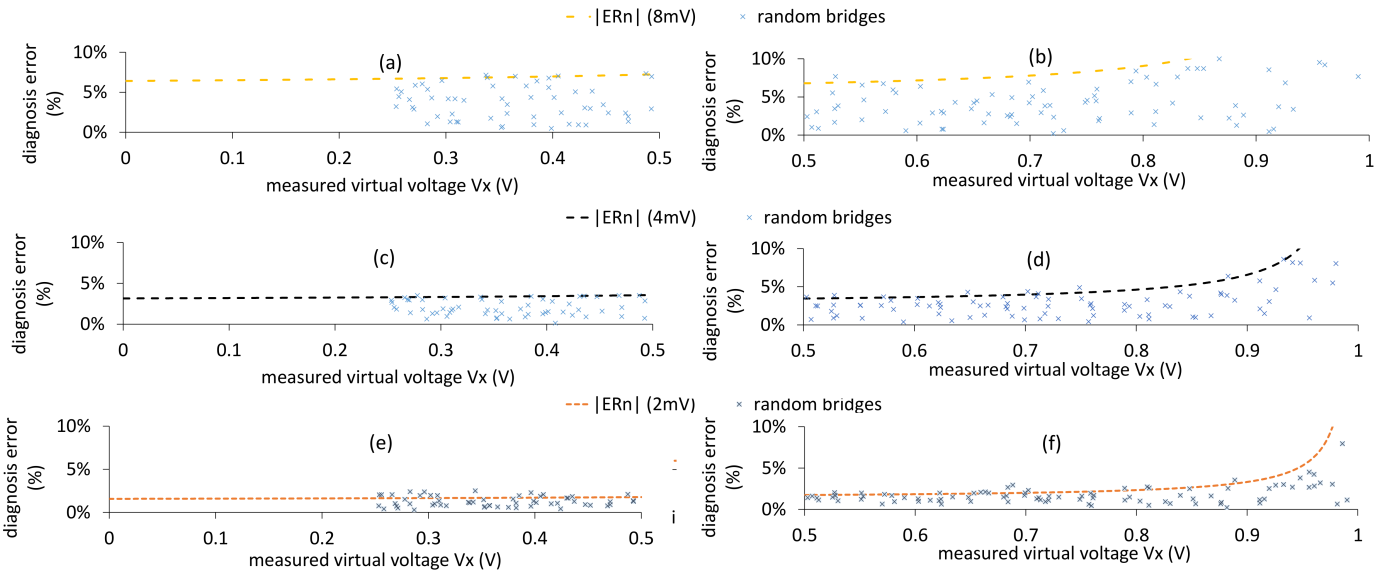

Fig. 14. Expected (ER_x) and actual ('x' points) diagnosis error for random bridges as a function of the measured virtual voltage (V_x) for sampling setups exhibiting a sampling error of (a)(b) 8mV; (c)(d)4mV; and (e)(f) 2mV; and bridges with (a)(c)(d) $V_{Vdd}@sb < V_{dd}/2$; and (b)(d)(f) $V_{Vdd}@sb > V_{dd}/2$

For each fault injection, we obtain an estimate R_{xi} together with the expected diagnosis error ER_{xi} by applying diagnosis Algorithm 1. The results for the s9234 benchmark are presented in Figure 14. For this case, we consider four sampling block setups with a voltage resolution $EV_x \approx 1, 2, 4$ and 8 mV. Figures 14(a) and (b) depict (using a dashed line) the expected diagnosis error $|ER_x|$ from (5) and the actual error (AER) of the resistive bridge estimation (labeled as 'random bridges' and using 'x' marks) evaluated as $\text{AER}_x = |R_{xi} - R_i|/R_i$. Recall that bridges exhibiting $V_{Vdd}@sb < 0.5$ V (Figures 14(a)) and $V_{Vdd}@sb > 0.5$ V (Figures 14(b)) are diagnosed using the VCO-N and VCO-P ring oscillators, respectively. We observe that only 8 points are higher than the $|ER_x|$ curve, exhibiting an actual error that is higher than expected. Thus, the accuracy, which is defined as $Acc = [1 - (\#\text{ iterations with AER} > \text{than } |ER|)/(\text{MC iterations})] \times 100$, and is found $Acc = 98\%$ for the examined case. Figures 14(c)(d) and (e)(f) present the results obtained by utilizing sampling block setups that perform with a voltage resolution $EV_x \approx 4$mV and 2mV, respectively. It is evident that only 12 and 28 bridges exhibit an error higher than expected, leading to a diagnosis accuracy of 97% and 93%, respectively, and that as the voltage error of the sensor reduces, the diagnosis accuracy also reduces. The diagnosis accuracy is lower than 100%, because the analytical model used for the sub-threshold leakage current is less accurate than the one used by SPICE. This accuracy loss could be used for improving the diagnosis estimation range given by eq. (5), however this way the proposed technique would require additional time-consuming SPICE simulations. As model-to-silicon discrepancies are inevitable, the provided numbers are an indication of their impact on the diagnosis accuracy. The proposed technique is sufficiently accurate and simple to fit the purpose of diagnosis.

A possible diagnosis result in a very large range, such as [0Ω 1GΩ], even if it might be 100% accurate, it might not be useful. Therefore, in addition to diagnosis accuracy, we evaluate the diagnosis resolution DR_n and DR_p by considering the average diagnosis estimation error, which is computed using (5) in the two voltage ranges $A_n = [0V,\ V_{dd}/2]$ and $A_p = [V_{dd}/2,\ V_{dd}]$, respectively:

$$DR_x = 1 - \frac{|\int_{A_x(1)}^{A_x(2)} ER_x dV_x|}{0.5V_{dd}} \tag{7}$$

The diagnosis resolution is obtained using the estimated diagnosis range, which can be useful to DFT engineers in order to avoid time-consuming SPICE simulations. In the next paragraph, the diagnosis accuracy of the estimated diagnosis range is evaluated using the actual diagnosis estimation error from SPICE results of the largest considered circuits and it is found to be higher than 94.5%.

We validate the proposed technique on the largest IWLS circuits [15], while considering various sampling setups (Section III-D3). The results are presented in Table III. The sampling time s in nanoseconds (ns) for each case is shown in column 's'. In column $|EI_x|(\%)$, we present for each case, the relative static power estimation error $|EI_x|$ of the proposed technique, evaluated using (6). In columns '$|ER_n|$ (%)' and '$|ER_p|$ (%)', we present the estimation error of the diagnosed effective resistance, evaluated using (5). For the '$|ER_n|$ (%)', the errors obtained at the corner voltage values $V_n = FF(V_{Vdd})$ and $V_n = 0.5$ V are presented (as in Figures 14(a)(c)(e)) and for the '$|ER_p|$ (%)', the errors obtained at the corner voltage values $V_p = 0.5$V and $V_p = 0.95$ V are presented (as in Figures 14(b)(d)(f)). The diagnosis error at the value of $0.95V_{Vdd}$ is for targeting bridges $R > 100\ \Omega$, because bridges $R \lesssim 100\ \Omega$ exhibit a very high $V_{Vdd}@sb$ and cannot be distinguished even with a sampling setup that performs with a voltage error of less than 0.1 mV. From Table III, we observe for the ethernet circuit that, as the sampling time s increases from 16 ns to 64 ns, the diagnosis resolution increases from 92.0% to 98.6%, because the estimation error of the leakage

TABLE III
POWER ESTIMATION ERROR (EI_x), DIAGNOSIS ERROR (ER_x), ACCURACY (ACC.), AND RESOLUTION (DR_x) ON A SET OF CIRCUITS

circuit	s (ns)	$\|EI_x\|$(%)		$\|ER_n\|$ (%)		$\|ER_p\|$ (%)		Acc. (%)	DR_x(%)	
		n	p	FF	0.5V	0.5V	0.95V		n	p
s9234	16	2.7	3.2	3.2	3.6	4.0	11.9	98.0	96.7	94.6
	32	1.4	1.6	1.6	1.8	2.0	6.0	97.0	98.3	97.3
	64	0.7	0.8	0.8	0.9	1.0	3.0	93.0	99.2	98.6
s5378	16	2.9	3.5	3.4	3.8	4.3	12.2	98.3	96.4	94.3
	32	1.5	1.8	1.7	1.9	2.2	6.2	97.3	98.2	97.1
	64	0.7	0.9	0.8	0.9	1.1	3.1	93.5	99.1	98.6
s13207	12.8	3.5	4.2	4.1	4.6	5.1	14.9	98.5	95.6	93.2
	25.6	1.8	2.1	2.0	2.3	2.6	7.6	97.5	97.8	96.5
	51.2	0.9	1.0	1.0	1.1	1.3	3.8	94.0	98.9	98.3
s38584	16	2.6	3.2	3.1	3.5	3.9	11.8	99.0	96.7	94.7
	32	1.3	1.6	1.5	1.7	2.0	6.0	97.8	98.4	97.3
	64	0.7	0.8	0.8	0.9	1.0	3.0	94.3	99.2	98.7
s38417	12.12	3.6	4.4	4.3	4.8	5.3	15.6	99.0	95.5	92.9
	24.24	1.8	2.2	2.1	2.4	2.7	8.0	98.0	97.8	96.4
	48.48	0.9	1.1	1.1	1.2	1.4	4.0	94.5	98.9	98.2
usb_funct	12.12	3.5	4.3	4.2	4.7	5.3	15.6	98.5	95.5	93.0
	24.24	1.8	2.1	2.1	2.3	2.7	7.9	97.8	97.8	96.4
	48.48	**0.9**	**1.1**	**1.0**	**1.2**	**1.3**	**4.0**	**94.5**	**98.9**	**98.2**
pci_bridge	12.12	3.5	4.3	4.2	4.7	5.2	15.6	99.3	95.6	93.0
	24.24	1.8	2.1	2.1	2.3	2.6	7.9	98.8	97.8	96.4
	48.48	**0.9**	**1.0**	**1.0**	**1.2**	**1.3**	**4.0**	**96.3**	**98.9**	**98.2**
ethernet	16	5.0	6.2	5.7	6.1	6.7	14.3	99.5	94.1	92.0
	32	2.5	3.0	2.8	3.0	3.4	7.3	99.0	97.1	95.9
	64	**1.3**	**1.5**	**1.4**	**1.5**	**1.7**	**3.7**	**98.0**	**98.6**	**97.9**

current at stand-by drops from 6.2% to 1.3%. At the same time the diagnosis accuracy, reduces slightly from 99.5% to 98%. Similar results are observed for all the examined circuits. For the largest circuits, marked with bold face in Table III, we conclude that the proposed technique achieves a diagnosis resolution higher than 98.6% and 97.9%, on weak and strong bridges, respectively, with a diagnosis accuracy that is greater than 94.5%.

D. Robustness of the sensor against process variation

We evaluate the impact of process variation on the variability of the virtual voltage at stand-by V_{Vdd}@sb, using Monte Carlo (MC) simulation. The width w, length l, threshold voltage V_{th} and effective mobility given by u_{eff} of each transistor follows a normal distribution around the nominal values, with a standard deviation $\sigma_Y = r \cdot Y_{nom}/3$, where Y_{nom} is the nominal values of the parameters w,l,V_{th} and u_{eff}, while r is the injected relative variability. Values $r = 10\%$ and 20% are considered. Using this setup, we perform 512 permutations, by conducting AC analysis of the circuit and measuring the $V_{Vdd}@sb$. The results for the s5378 circuit are shown in Figure 15. The $V_{Vdd}@sb$ ('y'-axis) is depicted for each MC permutation ('x'-axis). We observe that as the relative variability of the parameters increases from $r = 10\%$ (Figure 15(a)) to $r = 20\%$ (Figure 15(b)), the observed relative variability of the $V_{Vdd}@sb$, which is denoted as $r_V = 3 \cdot \sigma_V / \mu_V$, where μ_V the mean value of the observed $V_{Vdd}@sb$ and σ_V its standard deviation, slightly increases from 0.97% to 1.9%, respectively. We repeat the experiment, under the presence of bridging faults. For a bridge $R = 10\ M\Omega$, the r_V for $r = 10\%$ and 20% is found to be 0.12% and 0.53%, respectively, which is an order of magnitude lower compared to the variability of

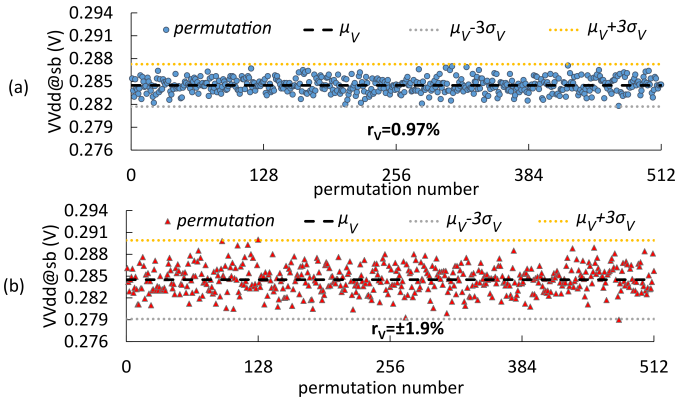

Fig. 15. Monte Carlo simulations for exploring the V_{Vdd}@sb variability induced by process variation for (a) $r = 10\%$; (b) $r = 20\%$

the fault-free case. For a bridge 100 Ω, the relative variability r_V for $r = 10\%$ and 20% is found to be 0.02% and 0.04%, respectively, which is two orders of magnitude lower compared to that of the fault-free case. Note that if this error is known, then it can be considered for improving the diagnosis estimation range. However, its computation requires Monte Carlo SPICE simulation, which might not be an option. The proposed technique is sufficiently accurate and simple to fit the purpose of diagnosis. Next, the diagnosis resolution loss is evaluated using the absolute sampling voltage error, which is less than 5.4 mV for the fault-free case, less than 1.32 mV for the medium-bridge case and less than 1 mV for the strong-bridge case. Even for the worst case, the diagnosis resolution DR_n is found to be greater than 96% and DR_p greater than 95%. Finally, a lower effect of the random variability on $V_{Vdd}@sb$ was observed for larger circuits. The proposed method does not stress the chip during the collection of the signature and the temperature variability is expected to be low. However, if temperature sensors are available during the signature collection and systematic temperature-induced variability is observed, then a similar approach as in [3] can be adopted for higher accuracy.

To minimize the impact on the power consumption and performance of the circuit, the on-chip power-networks sensor (Section III-C) is placed in a separate power-gated domain. This is achieved using additional power switches connected to the power supply and to the ground rail, together with a transmission gate connected to the virtual-voltage rail (Figure 7(b)). The limitation of this solution is that it implies additional physical constraints during layout for the extra power-gated domain, which can be addressed by automated physical synthesis tools. It should be noted that this unit is small and can be placed manually. Another limitation of the proposed technique is that it exhibits high diagnosis error for circuits that suffer from strong-bridges (Figures 12 and 14), because their $V_{Vdd}@sb$ can be similar to their operating voltage V_{dd}.

V. CONCLUSIONS

We demonstrated that stuck-ON faults on the power switches and resistive bridges between the power networks can impair the power saving capability of power-gating designs

(Figure 2 and Table I). For grading the magnitude of such defects that can negatively affect the power saving of power gating designs, we proposed a diagnosis technique of bridges between the power networks (Section III). The proposed technique utilizes an on-chip power-networks sensor (Figure 7) and a low-cost signature generation logic (Figure 10) for collecting a signature that is sensitive to the voltage of the circuit's power-networks at stand-by. A novel algorithm (Algorithm 1) processes the collected signature for diagnosing resistive bridge between the power networks at stand-by and its impact on the static power consumption. We demonstrated a trade-off between area and voltage monitoring resolution achieved by the signature generation unit (Figure 13), and we evaluated its area cost (Table II) and its diagnosis resolution (Table III) on a set of the largest IWLS benchmarks [15]. It performs with a resolution that is greater than 97.9% and with a scalable area cost of 0.3% compared to a design with 157K gate equivalents. The accuracy of the proposed technique was validated through SPICE simulation (Figure 14) and its robustness to process variation through Monte Carlo simulation (Figure 15).

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